REMARKS

I. STATUS OF THE CLAIMS

New claim 50 is added herein. Support for the new claim is found, for example, on page 19, lines 21-34, of the application.

In view of the above, it is respectfully submitted that claims 1-36, 49 and 50 are currently pending.

II. ELECTION / RESTRICTIONS UNDER 37 C.F.R. § 1.142

Claim 49 stands withdrawn from consideration as being directed to a non-elected invention. The Examiner maintains the restriction requirement in the Advisory Action, stating that "Means plus function language used in claim 49 is referring to an apparatus, while claim 1 'ing language is referring to steps. Therefore, they are different inventions." See page 2, lines 1-3, of the Advisory Action. However, the restriction requirement is improper per the following.

The Examiner may require a restriction if two or more "independent *and* distinct" inventions are claimed in one application. See MPEP § 802.01. The term "independent" means that there is no disclosed relationship between the two inventions claimed. See MPEP § 802.01(I). The inventions must be *unconnected* in design, operation and effect. See *Id.* For instance, a process and an apparatus incapable of being used to practice the process are independent inventions. See *Id.* Two or more inventions are "related (i.e., not independent) if they are disclosed as connected in at least one of design (e.g., structure or method of manufacture), operation (e.g., function or method of use), or effect. Examples of related inventions include combination and part (subcombination) thereof, process and apparatus for its practice, process and product made, etc."

The Examiner states in the December 8, 2006 Office Action that claim 49 is "independent *or* distinct" from the invention originally claimed. The Applicant respectfully points out that the MPEP requires that two inventions must be independent *and* distinct in order for a restriction requirement to be proper. Claim 49 is similar to claim 1, but is written in Means Plus Function format. See MPEP 2181 and 35 U.S.C. § 112 ¶ 6. Claim 49 replaces the detecting, calculating and correcting language from claim 1 with a means for detecting, means for calculating and a means for correcting. Method and apparatus claims are permissible in the same application. Further, some embodiments of the apparatus as recited in claim 49 could practice the method as recited in claim 1. Thus, the invention recited, for example, in claim 1 and the invention recited,

for example, in claim 49 are clearly not "independent and distinct" as is required for a proper restriction requirement by Chapter 800 of the MPEP.

In view of the above, it is respectfully submitted that claim 49 is not independent and distinct from the invention as claimed in claim 1 and no election/restriction should apply. The applicant respectfully requests that the election/restriction be withdrawn.

III. REJECTION UNDER 35 U.S.C. § 102(b) OF CLAIMS 1-2, 4-8, 11-13, 15 AND 17 AS BEING ANTICIPATED BY LEEDY (US 5,103,557)

Claim 1 recites "calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and holding said displacement as first displacement data." See Claim 1 and, for example, page 11, lines 2-6, of the application. Leedy fails to anticipate the present invention under 35 U.S.C. § 102(b).

Leedy discloses using a tester surface to bring a wafer within a few mils of said tester surface using the pressure of a fluid, separating the tester surface and the wafer, and makes a first approximation of the contact points through a conventional optical aligner. See column 4, line 66 through column 5, line 11, of Leedy. The alignments are determined by using alignment patterns in predetermined positions on both the wafer being tested and the tester surface. See column 5, lines 3-7, of Leedy. The data from the Leedy invention lists the location of the defective transistors or ICLUs. See column 5, lines 33-35, of Leedy. The CAD means then works out an interconnect strategy, forming a net list of interconnect patterns to bypass defective ICLUs by interconnecting defect-free ICLUs from a stock of redundant ICLUs. See column 5, lines 37-43, of Leedy.

Conversely, the present invention as recited in amended claim 1 calculates the *displacement* between the design position and the actual position of the component. See Claim 1 and, for example, page 11, lines 2-6, of the application. Leedy only lists the *location* of *defective* transistors or ICLUs. See column 5, lines 33-35, of Leedy. Displacement can be defined as "the linear or angular distance in a given direction between a body or point and a reference position." See Dictionary.com, http://dictionary.reference.com/browse/displacement, Lexico Publishing Group (2007). On the other hand, location can be defined as "a point or extent in space." Dictionary.com, http://dictionary.reference.com/browse/location, Lexico Publishing Group (2007). As such, a location is a point whereas a displacement is a distance.

Because Leedy only determines which transistors and ICLUs are not accurately aligned

per the CAD master placement scheme and interconnects redundant ICLUs to replace them, it never determines the displacement between the design position and the actual location of the component. See column 5, lines 3-43, of Leedy. Further, there is no need in the present invention as recited, for example, in claim 1, for the electronic components to be defective.

Claim 1 recites "correcting, based on said first *displacement data* [emphasis added], design data to be used for processing said board after said board is covered with said first insulating layer to form a wiring pattern connected to said first electrical component." See Claim 1 and, for example, page 11, lines 2-5, page 14, lines 16-35, and Figs. 7 and 8, of the application. The Examiner stated in the Advisory Action that because "the CAD means then, by special software algorithms works out an interconnect strategy for each die" (col. 5, lines 35-39) after creating a list of the locations of defective transistors, that "[t]his anticipates that the software calculates a displacement between the design position of the first electronic component and the actual position of the first electronic component on the surface of the board." See page 2, lines 3-9, of the Advisory Action.

However, the software in Leedy never calculates a displacement and there is neither a need nor a motivation for it to do so. The alignments are determined by using *alignment patterns* in predetermined positions on both the wafer being tested and the tester surface. See column 5, lines 3-7, of Leedy. The CAD means then works out an interconnect strategy, forming a net list of interconnect patterns to bypass defective ICLUs by interconnecting defect-free ICLUs from a stock of redundant ICLUs. See column 5, lines 37-43, of Leedy. Thus, Leedy only determines whether the component is in a predetermined position using the alignment pattern. The actual position is never known. Because Leedy never calculates the displacement between design data and the actual location of a component, it cannot make corrections based on displacement data.

The above comments are specifically directed to claim 1. However, it is respectfully submitted that the comments would be helpful in understanding various differences of various other claims over the cited reference.

In view of the above, it is respectfully submitted that the rejection is overcome.

IV. REJECTION UNDER 35 U.S.C. § 103(a) OF CLAIMS 19-20, 22-26 AND 29-36 AS BEING UNPATENTABLE OVER LEEDY (US 5,103,557) IN VIEW OF KULKARNI ET AL (US 5,991,699).

Claim 19 discloses "calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component detected from first image data obtained by imaging the surface of said board, and holding said displacement as first displacement data." See Claim 19 and, for example, page 11, lines 2-6, of the application. Per the above, Leedy fails to disclose calculating the displacement between the design position and the actual position of a component.

The above comments are specifically directed to claim 19. However, it is respectfully submitted that the comments would be helpful in understanding various differences of various other claims over the cited reference.

In view of the above, it is respectfully submitted that the rejection is overcome.

Claims 14, 16 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leedy (US 5,103,557) in view of Kulkarni et al (US 5,991,699).

Claims 14, 16 and 18 depend from claim 1, adding further limitations thereto. Per the above, Leedy fails to disclose calculating the displacement between the design position and the actual position of a component.

In view of the above, it is respectfully submitted that the rejection is overcome.

VI. CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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